REMARKS

This is intended as a full and complete response to the Office Action dated March 14, 2006 (hereinafter "the Office Action") having a shortened statutory period for response set to expire on June 14, 2006.

Claims 1-2 and 4-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Application Publication No. 2003/0163298 ("Odom") in view of U.S. Patent No. 6,847,654 ("Zegelin") and further in view of U.S. Application Publication No. 2002/0101848 ("Lee"). With this rejection, Applicants respectfully disagree, at least for the reasons set forth below.

Reliance in the Office Action on Fig. 3B of Odom is misplaced for at least the following reasons. First, Odom does not teach the feature that the transceiver and programmable gates are formed as an integrated circuit as claimed in amended claims 1 and 7. The reconfigurable I/O ("RIO") card 110F of Fig. 3B of Odom has multiple separate integrated circuits, where programmable hardware 106 is separate from what the Office Action has indicated as being a transceiver in Odom, namely I/O connector 202. Odom does not teach the incorporation of I/O connector 202 into programmable hardware 106. Having a more closely coupled transceiver and medium access layer may facilitate enhanced performance or reduced power consumption.

Secondly, Odom does not teach the feature of coupling the transceiver to the programmable gates through programmable input/output blocks, as claimed in amended claims 1 and 7. If I/O connector 202 is a transceiver as alleged in the Office Action, then such transceiver is coupled to programmable hardware 106 via fixed hardware resources 204 of Odom. Odom indicates that I/O connector 202 may be fixed like fixed hardware resources 204, and goes on to emphasize that the physical I/O is static. (See Odom, from [0209] to [0210].) As Odom teaches using fixed hardware resources 204 for coupling programmable hardware element 106 to a physical I/O, Odom teaches away from using programmable input/output blocks for coupling to a transceiver.

Moreover, reliance in the Office Action on Zelegin is misplaced. Zegelin does not teach having a common access as claimed in amended claims 1 and 7. Rather FIG. 2 of Zegelin shows going from lower MAC 150 to upper MAC 210 prior to reaching I/O 220. As indicated in Zegelin at col. 5, lines 1-6, this means that information regarding upper MAC 210 must be incorporated into the process of lower MAC 150. In contrast, the medium access layers and the data-link layer have the capability to share a common access feature as claimed, and thus need not be limited like Zelegin.

In the Office Action, Lee is used for the limited purpose of reference with a baseband controller and various communications standards. In order to advance prosecution, Applicants accept Lee for this limited purpose.

For any of the several above-mentioned reasons, it is respectfully submitted that the combination of Odom, Zelegin, and Lee, even if proper which, as shall be argued below, it is not, does not show, describe, or suggest all of the features of amended claims 1 and 7. Thus, it is Applicants' position that claims 1 and 7 should be allowable over the reference of Odom in combination with Zelegin and Lee. Furthermore, claims 5, 6, and 8-10, which either directly or indirectly depend upon an allowable base claim 1 or 7, likewise should be allowable. Even though claims 2 and 4 have been canceled without prejudice, reference is made to those claims owing to subject matter thereof being incorporated into claim 1.

It is now well established that the Patent Office bears the burden of establishing a *prima facie* case to maintain a rejection for obviousness. Failure to make such a *prima facie* showing by the Patent Office is to result in a withdrawing of the rejection.

The MPEP states what the Patent Office considers to be a "*prima facie* case" of obviousness at Section 706.02(j). Taking *arguendo* the Patent Office criteria of a "*prima facie* case" of obviousness as the standard, it will become apparent that the instant rejection for obviousness fails to meet such criteria and, accordingly, that the rejection of claims 1-2 and 4-10 for obviousness is improper and should be withdrawn with respect to the remainder of those claims still pending.

According to the Patent Office, the first element of a *prima facie* case for obviousness is that there must be some suggestion or motivation to modify a reference or combine the teachings of the references. This suggestion must come from either of the references or be knowledge generally available to one of ordinary skill in the art.

Nothing in the Office Action indicates that there is any suggestion in any of the references of Odom, Lee and Zelegin for this combination. Thus, the combination cannot rest upon any suggestion in any of these references.

Moreover, it is Applicants' position that the basis for the combination as stated in the Office Action provides no reasonable basis for the assertion that one of ordinary skill in the art would be led to combine these particular references of Odom, Zelegin, and Lee. Merely because a collection of communication standards may exist among the cited references, does not provide legally sufficient suggestion for the modification of Odom with Zelegin and Lee.

According to the Patent Office, the second element of a *prima facie* case for obviousness is that there must be a reasonable expectation of success. In order to ascertain whether there would be such a reasonable expectation of success, there must be some understanding of how the primary reference of Odom is to be modified by the secondary references of Zelegin and Lee to arrive at the claimed invention.

Presently, the indication in the Office Action is that Odom is to be modified with the upper and lower MAC division of Zelegin to support communication standards disclosed in Lee and Zelegin. However, as indicated above, Zelegin does not describe a common access for MACs to a transceiver. Moreover, in Fig. 3B of Odom, there is no indication of a common access as claimed. Thus, even if the combination was appropriate, which it is not, it would not result in the invention as claimed for example in amended claims 1 and 7.

According to the Patent Office, the third element of a *prima facie* case for obviousness is that the cited prior art references must teach or suggest all the claim limitations. However, as indicated in the arguments raised above, features as claimed

in claims 1 and 7 are not taught or suggested by the Odom, Zelegin, and Lee references.

Thus, it is respectfully submitted that the rejection of claims 1-2 and 4-10 under 35 U.S.C. § 103(a) as being obvious over Odom in view of Zelegin and Lee is improper and should be withdrawn for any of the reasons provided above.

Claims 3 and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Odom in view of Zelegin and Lee, and further in view of U.S. Pat. No. 6,212,190 ("Mulligan"). In this rejection, Mulligan is added to the combination Odom, Zelegin, and Lee for the limited purpose of disclosing TDMA. While Applicants accept that TDMA is known, Applicants respectfully disagree with the rejection of claims 3 and 11 for any of the above-mentioned reasons in response to the rejection of claims 1-2 and 4-10, which are hereby applied to this rejection of claims 3 and 11. Moreover, claims 3 and 11, which either directly or indirectly depend upon an allowable base claim 1 or 7, should likewise be allowable. Furthermore, it is respectfully submitted that the rejection of claims 3 and 11 under 35 U.S.C. § 103(a) as being obvious over Odom in view of Zelegin, Lee, and Mulligan is improper and should be withdrawn for any of the reasons provided above with regard to the combination of Odom in view of Zelegin and Lee.

Claims 12-17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Application Publication No. 2002/0094087 ("Dellmo"). With this rejection, Applicants respectfully disagree, at least for the reasons set forth below.

In Dellmo, the MAC is external to each instance of an FPGA in each of the figures. For example, in Fig. 7 of Dellmo, MAC 60 is external to FPGA 74. In FIG. 9 of Dellmo, MAC 60 is external to FPGA 74. In Fig. 10 of Dellmo, MAC 60 is external to FPGA 74. Notably, in the Office Action the entire cryptography circuit 70 is mistaken for FPGA 74 with reference to Fig. 7 of Dellmo.

Furthermore, in Fig. 7 of Dellmo, a cryptographic processor 72 is indicated as being external to FPGA 74. Later, at Fig. 9 of Dellmo, cryptographic processor 72 is indicated as a palisades ASIC 72, and likewise in Figs. 10 and 11 of Dellmo, the cryptographic processor is a palisades ASIC 72. Palisades ASIC 72 in each of these

figures of Dellmo is separate from FPGA 74 of Dellmo. Notably, in the Office Action, the palisades ASIC 72 of Dellmo is mistaken for programmable configuration logic blocks.

In view of these few clarifications of the Dellmo reference, claim 12 cannot possibly be obvious in view of Dellmo. For example, in claim 12, the FPGA comprises programmable configuration logic blocks; and thus the programming instructions for the programmable configuration logic blocks to be configured yield devices internal to the FPGA. Accordingly, the radio interface and controller, the medium access control protocol engine and configuration controller, and the baseband processor interface would be instantiated in programmable configuration logic blocks internal to the FPGA. In contrast to Fig. 7 of Dellmo for example, MAC 60 is not described as being in programmable configuration logic blocks and is not described as being internal to FPGA 74.

Claims 13-17, in addition to being allowable as dependent from an allowable base claim, should each be allowable on their own in view of Dellmo for the following reasons. Claim 13 indicates that a baseband processor is instantiated in the programmable configuration logic blocks of the FPGA. In contrast to claim 13, Fig. 7 of Dellmo shows baseband processor 51 as being external to FPGA 74. In contrast to Dellmo, claim 14 indicates that an encryption engine is instantiated in the programmable configuration logic blocks of the FPGA. In Fig. 7 of Dellmo, cryptographic processor/palisades ASIC 72 is shown external to FPGA 74.

Claims 15 and 16 each recite a host bus interface feature, and claims 16 and 17 each recite a host device controller feature. Applicants respectfully disagree with the interpretation of Dellmo as advanced in the Office Action. Applicants do not understand Dellmo as providing any reference to a host bus interface or host device controller as alleged in the Office Action. Rather, Dellmo in Fig. 7 shows that a peripheral bus, or more particularly a PCMCIA connector 27, is used. This connector is on the MAC side, not on the host side.

Moreover, the suggestion in the Office Action that use of a LAN for selecting between a host device interface and a host device controller as claimed in claim 17

fails to account for at least two things. First, a LAN connection on the MAC side and is not on the host side. Secondly, the host bus interface and host device controller are in programmable configurable logic as claimed, and not computer and user stations as suggested in the Office Action.

Additionally, Applicants respectfully disagree with the assertion in the Office Action that using memory for storing cryptographic information as in Dellmo somehow renders obvious the features of program memory with programming instructions for configuring programmable configuration logic blocks of the FPGA as: a radio interface and controller; a medium access control protocol engine and configuration controller; and a baseband processor interface. First, the two fields are non-analogous. Cryptography is not related to configuration information for programmable configurable logic. Not only are they different fields, they are directed at different problems. Paragraph [0055] of Dellmo as referenced in the Office Action is drawn to tamper proofing the cryptographic information, which if tampered would render the cryptographic information unusable. This is problem in Dellmo is different from the issue of supporting multiple types of communication formats.

Moreover, Fig. 10 of Dellmo as referenced in the Office Action, shows that FPGA 74 includes in large part a serial control interface between MAC 60 and palisades ASIC 72. Applicants strongly disagree with any notion that a serial interface, which may be used for a MAC in an FPGA means anything other than having a serial interface in an FPGA. Applicants believe that such serial interface certainly does not provide any suggestion for instantiating in programmable configurable logic of an FPGA a device capable of serial communication.

Applicants respectfully believe at least for the reasons set forth above that claims 12-17 should be allowed in plain view of Dellmo, and accordingly request that the rejection of claims 12-17 be withdrawn.

On December 19, 2005 along with the response to the First Office Action, Applicants filed a Supplemental Information Disclosure Statement citing two additional references. The Substitute for 1449A/PTO filed with the IDS has not yet been returned initialed by the examiner indicating his consideration. Applicants hereby

request the examiner consider the two references and return an initialed copy of the 1449.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the Applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on June 8, 2006.

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